ADS1256EVM Evaluation Module

This user's guide describes the characteristics, operation, and use of the ADS1256EVM. This EVM is an evaluation fixture for the ADS1256 24-bit delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS1256EVM is designed for prototyping and evaluation. It also serves as an evaluation platform for the ADS1255, which is a proper subset of the ADS1256. A complete circuit description, schematic diagram, and bill of materials are included. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1256EVM.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Device	Literature Number
ADS1256	SBAS288
REF5025	SBOS410
OPA350	SBOS099

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1 ADS1256EVM Overview

The ADS1256EVM is an evaluation fixture for the ADS1256 24-bit delta-sigma ADC.

1.1 Introduction

Many data converter evaluation fixtures contain a computer interface or a microcontroller, but the ADS1256EVM contains only the ADS1256 device and a few support components. All ADS1256 pins are accessible through various pins on the ADS1256EVM analog and digital connectors.

The ADS1256EVM is designed using a simple card format developed by TI. This simple, consistent design makes the ADS1256EVM very easy to connect to your own prototype system. You can even think of the ADS1256EVM as an alternate package for the ADS1256—one much larger than the device itself, but also much easier to wire up by hand on your test bench.

The ADS1256EVM can be plugged directly into suitable motherboards, such as the HPAMCU Interface Board for use with an MSP430 microcontroller or the 5-6K Interface Board for use with TMS320 Series DSP Starter Kits. See TI's web site for example code using the ADS1256EVM with the MSP430F449.

The ADS1256EVM, together with a motherboard and appropriate software, also forms a complete evaluation system for verifying the performance of the ADS1256; see the ADS1256 product information folder on the Texas Instruments web site for more information.

If you intend to use the ADS1255 in your application, use the ADS1256EVM for evaluation and test purposes. The ADS1255 is in a smaller package, and lacks inputs AIN2 through AIN7; otherwise, it is identical to the ADS1256.

1.2 Built-In Accessories

The ADS1256EVM includes a system clock crystal and a low-noise voltage reference. Both are optional; you can select an external system clock and an external reference using slide switches.

The +2.5V reference circuit is based on a REF5025 buffered by an OPA350 and filtered by a large tantalum electrolytic capacitor. While its noise performance is not sufficiently low to allow the ADS1256 to perform at its lowest noise level at all data rates, it can closely approach the limit, and is representative of the kind of reference circuit used in many applications.

1.3 Connectors

The ADS1256 device on the ADS1256EVM is connected through four headers: the analog connector, the serial connector, the power connector, and the GPIO header. Pinouts and locations for the connectors are given in this section.

The **analog connector** (J1) carries analog I/O. The ADS1256 has a nine-input multiplexer connected through pins 1 through 8 and 10. An optional external differential reference can be connected to pins 18 and 20.

The **serial connector** (J2) carries the ADS1256 serial digital interface, an optional external system clock signal, and an I^2C connection to the onboard serial EEPROM.

The **power connector** (J3) carries the power supplies. The ADS1256EVM requires a +5V analog supply and a +1.8V to +3.3V digital supply. The board is designed using a single ground net connected to DGND. An AGND pin is also provided; it can be connected to DGND using jumper J4.

The **GPIO header** (J5) provides a connection to the four GPIO pins on the EVM.

The ADS1256 uses separate supplies for its analog and digital sections. A jumper is inserted in each supply line. These jumpers allow the current of each supply to be measured independently.

1.4 Controls

The ADS1256EVM is configured using four slide switches and a jumper.

Switches S1 and S2 select the input signal provided to the first four multiplexer inputs on the ADS1256. Normally you will use the external input, but you can also use the switches to short the inputs together and to connect the reference voltage to the inputs. Additionally, the latter two positions are useful for conducting noise and functional tests.

Switch S3 selects the reference input. One position selects the external reference input pins on the analog connector (J1). The other two positions connect the onboard +2.5V reference in one of two ways: between ground and the reference, or between the reference and the analog supply.

Switch S4 selects the system clock source for the ADS1256. You can select between the onboard 7.68MHz crystal or an external clock.

1.5 Setting Up

The ADS1256EVM is configured according to its use. Thus, there is no single correct procedure to configure the test fixture.

Nevertheless, it is useful to remember the following things when you are setting up the board:

- If you are not measuring the ADS1256 supply current, remember to place shorting blocks in the appropriate positions on jumper block J4. Without these shorting blocks, the ADS1256 will not be powered on, and the device will not work properly.
- Unless you are using two entirely separate power supplies for analog and digital, place a shorting block on the analog-digital ground jumper. This block connects the analog and digital grounds together, which is the normal way to operate the ADS1256EVM.
- Check the system clock switch. If it is set to *EXT* and you have not connected a clock signal to the external clock input pin on J2 pin 17, the ADS1256 will not operate.
- The RESET and $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ pins (J2 pins 14 and 19) can be configured for GPIO control by a host processor when jumpers J6 and J7 are properly configured. J6 controls the $\overline{\text{SYNC}}$/PWDN. A shunt placed on J6 pins 1-2 ties the $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ input to the digital supply. Placing a shunt on J6 pins 2-3 applies a pull-down resistor to the input and allows GPIO control through J2 pin 19. J7 can be used to supply a logic high to the RESET pin (shunt on J7 pins 2-3) or GPIO input from a host processor via J2 pin 14 (shunt on pins 1-2). See the ADS1256 data sheet for further information about the $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ pin functionality.

2 Circuit Description

This section describes the connectors, controls, and circuit design of the ADS1256EVM in detail.

2.1 I/O Connectors and Testpoints

The positions and functions of the connectors and testpoints are shown in Figure 1.

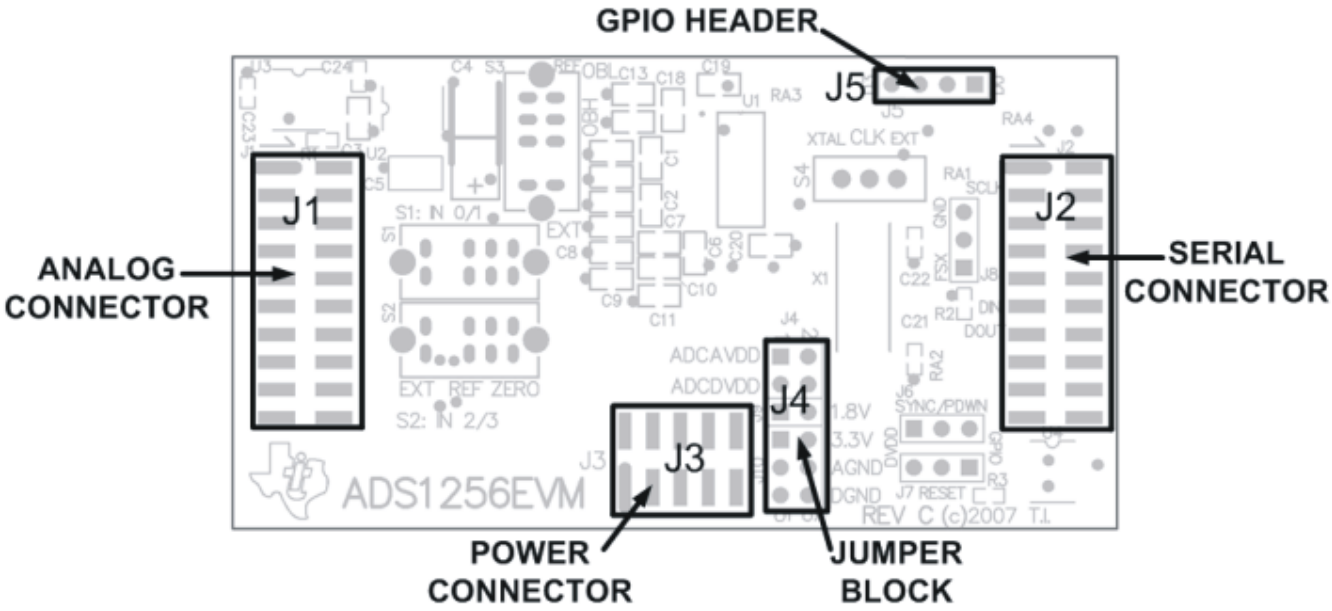


Figure 1. Connectors and Jumpers

Many of the pins on the connectors are not used. On the pinout diagrams, unused pins are not marked. In the pin description tables, unused pins are not listed, and ground pins are listed together, with the exception of the power connector.

J1, J2, and J3, although each treated as a single connector, are actually mounted as connector pairs in a pass-through configuration. Each pair has a surface-mount header on the top (component) side of the board, and a corresponding surface-mount socket on the bottom (solder) side of the board. The headers, mounted on top, are suffixed **A**; the sockets, mounted on bottom, are suffixed **B**.

In the schematic, the connector pairs are shown as one symbol. For J1, J2, and J3, all bottom-side pins are connected to the corresponding top-side pins; for example, J1B pin 1 connects to J1A pin 1, J1B pin 2 connects to J1A pin 2, etc. This convention holds true for every pin on connectors J1, J2, and J3.

In the following descriptions, the connector pairs will be referred to as a single connector.

2.1.1 J1: Analog Connector

The analog connector pinout is shown in Figure 2 and described in Table 1.

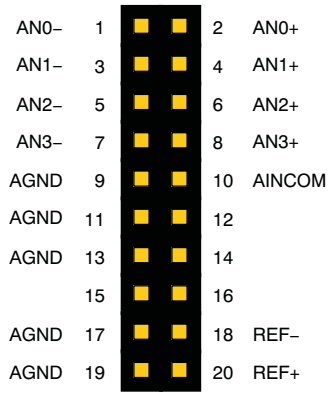


Figure 2. Analog Connector Pinout

CAUTION

Although certain pins are described as *negative*, never apply voltages less than –0.3V to these pins. The ADS1256 is not a bipolar-input device, and it cannot accept negative voltages below –0.3V without damaging the functional operation of the unit.

The negative input pins are so named because the voltage on such a pin is subtracted from a positive input pin during a reading.

Table 1. Analog Connector Pin Descriptions

Pin Number	Pin Name	Standard Name	Direction	Function
1	AIN0	AN0–	Input	Analog input 1 (switched by S1)
2	AIN1	AN0+	Input	Analog input 0 (switched by S1)
3	AIN2	AN1–	Input	Analog input 3 (switched by S2)
4	AIN3	AN1+	Input	Analog input 2 (switched by S2)
5	AIN4	AN2–	Input	Analog input 4
6	AIN5	AN2+	Input	Analog input 5
7	AIN6	AN3–	Input	Analog input 6
8	AIN7	AN3+	Input	Analog input 7
10	AINCOM	AN4+	Input	Analog input common
18	SYSREFN	REF–	Input	Inverting external reference input
20	SYSREFP	REF+	Input	Noninverting external reference input
9, 11, 13, 17, 19	GND	AGND	Power	Signal ground

2.1.2 J2: Serial Connector

The serial connector pinout diagram is shown in Figure 3 and described in Table 2.

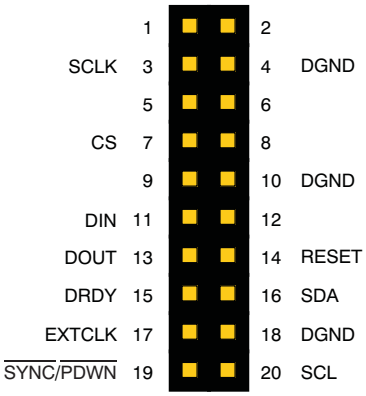


Figure 3. Serial Connector Pinout

Table 2. Serial Connector Pin Descriptions

Pin Number	Pin Name	Standard Name	Direction	Function
3	SCLK	CLKX	Input	Serial clock input
7	CS	FSX	Input	Chip-select (via J8)
11	DIN	DX	Input	Serial clock input
13	DOUT	DR	Output	Serial data output
14	RESET	GPIO4	Input	Reset input (via J7)
15	DRDY	INT	Output	Data ready signal
16	SCL	SCL	I/O	I^2C clock line
17	EXTCLK	TOUT	Input	External system clock input
19	$\overline{\text{SYNC}}/\overline{\text{PDWN}}$	GPIO5	Input	Synchronization and power down control pin (via J6)
20	SDA	SDA	I/O	I^2C data line
4, 10, 18	GND	DGND	Power	Signal ground

2.1.3 J5: GPIO Header

The ADS1256 has four general-purpose I/O (GPIO) pins. One of these pins can also be configured as a buffered system clock output. This output is typically used to clock additional ADS1255/ADS1256 devices, but can be used for other purposes.

Each pin is connected to the GPIO header through a 100Ω resistor. 100kΩ pull-downs on each pin protect the GPIOs when they are configured as inputs, which is the default setting.

The GPIO header pinout diagram is shown in Figure 4 and described in Table 3.

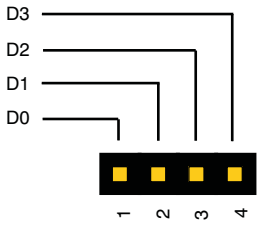


Figure 4. GPIO Header Pinout

Table 3. GPIO Pin Descriptions

Pin Number	Pin Name	Function
1	D0	GPIO or Buffered system clock output
2	D1	GPIO
3	D2	GPIO
4	D3	GPIO

2.1.4 J3: Power Connector

The power connector pinout diagram is shown in Figure 5 and described in Table 4.

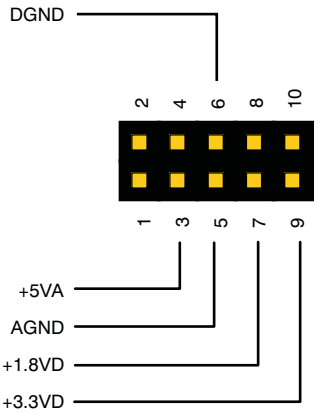


Figure 5. Power Connector Pinout

Table 4. Power Connector Pin Descriptions

Pin Number	Pin Name	Function	Use on ADS1256EVM
1	+VA	Positive Analog Supply, +5V to +18V	Not used
2	–VA	Negative Analog Supply, –5V to –18V	Not used
3	+5VA	Positive Analog Supply, +5V	Analog supply
4	–5VA	Negative Analog Supply, –5V	Not used
5	AGND	Analog Ground	Optional connection to DGND through J4
6	DGND	Digital Ground	Ground
7	+1.8VD	Positive Digital Supply, +1.8V	Digital supply; select using J4
8	VD1	Positive Digital Supply	Not used
9	+3.3VD	Positive Digital Supply, +3.3V	Digital supply; select using J4
10	+5VD	Positive Digital Supply, +5V	Not used

The ADS1256 uses an analog supply of +5V and a digital supply of +1.8V to +3.3V. Both +1.8V and +3.3V are available as standard supply voltages over the power connector, and the ADS1256EVM allows you to switch between them using J4.

2.2 Jumpers

There are six jumpers on the ADS1256EVM, arranged in a single jumper block. The pinout of this jumper block is shown in Figure 6.

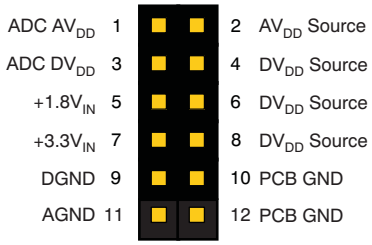


Figure 6. Jumper Block

2.2.1 J4 Pins 1–2: ADS1256 Analog Power Supply

This jumper can be used to measure the current of the ADS1256 analog power supply.

For normal operation, this jumper should be shorted.

2.2.2 J4 Pins 3–4: ADS1256 Digital Power Supply

This jumper can be used to measure the current of the ADS1256 digital power supply.

For normal operation, this jumper should be shorted. The voltage of the digital supply is chosen by the jumper on pins 5–6 (1.8V) or 7–8 (3.3V).

2.2.3 J9 Pins 1–2: Select 1.8V Digital Supply Voltage

These pins select 1.8V for the digital supply voltage. If this selection is used, do not populate pins 7-8.

2.2.4 J10 Pins 1–2: Select 3.3V Digital Supply Voltage

These pins select 3.3V for the digital supply voltage. If this selection is used, do not populate pins 5-6.

2.2.5 J10 Pins 3–4: DGND Select

Shorting this jumper connects the ADS1256EVM ground net to DGND.

2.2.6 J10 Pins 5–6: AGND Select

Shorting this jumper connects the ADS1256EVM ground net to AGND.

2.3 Switches

The positions and functions of the EVM switches are shown in Figure 7.

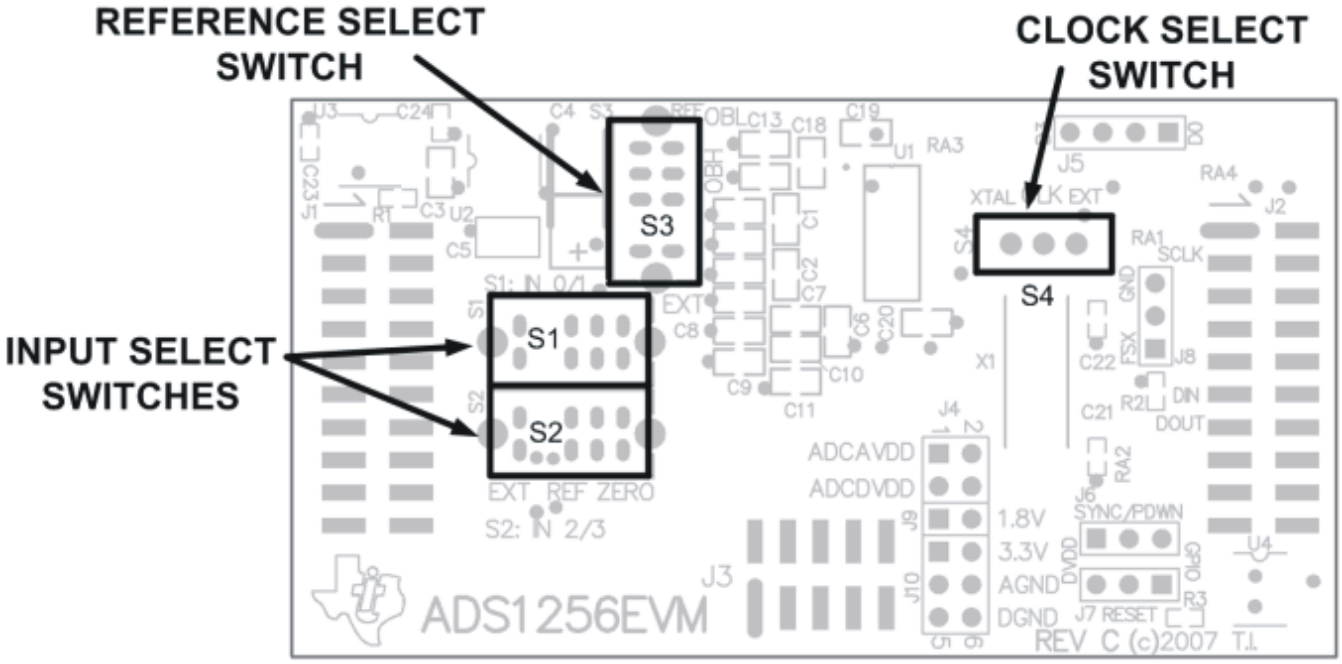


Figure 7. Switches

2.3.1 S1: AIN0–1 Input Select

These switches control which lines are routed to the ADS1256 AIN0–AIN1 inputs. The positions of the switches are described in Table 5.

Table 5. AIN0–1 Input Select Switch (S1)

Board Marking	Switch Position	Input Source	AIN0 Connection	AIN1 Connection
EXT	Left	External (J1, pins 1 and 2)	J1 pin 2	J1 pin 1
REF	Middle	Reference voltage	+2.5V	Ground
ZERO	Right	Zero (shorted to reference)	+2.5V	+2.5V

In the EXT position, J1 pins 1 and 2 are connected to the ADS1256 AIN1 and AIN0 pins, respectively.

In the REF position, the reference is connected across the ADS1256 AIN0 and AIN1 pins.

In the ZERO position, both AIN0 and AIN1 are connected to the reference. This gives a zero-scale reading across AIN0 and AIN1.

The REF and ZERO positions are useful for noise tests.

2.3.2 S2: AIN2–3 Input Select

These switches control which lines are routed to the ADS1256 AIN2 through AIN3 inputs. The positions of the switches are described in Table 6.

Table 6. AIN2–3 Input Select Switch (S2)

Board Marking	Switch Position	Input Source	AIN2 Connection	AIN3 Connection
EXT	Left	External (J1, pins 3 and 4)	J1 pin 4	J1 pin 3
REF	Middle	Reference voltage	+2.5V	Ground
ZERO	Right	Zero (shorted to reference)	+2.5V	+2.5V

In the EXT position, J1 pins 3 and 4 are connected to the ADS1256 AIN3 and AIN2 pins, respectively.

In the REF position, the reference is connected across the ADS1256 AIN2 and AIN3 pins.

In the ZERO position, both AIN2 and AIN3 are connected to the reference. This gives a zero-scale reading across AIN2 and AIN3.

The REF and ZERO positions are useful for noise tests.

2.3.3 S3: Reference Input Select

This switch controls which signals are connected to the differential reference input on the ADS1256. The positions of the switch are described in Table 7.

Table 7. Reference Input Select Switch

Board Marking	Switch Position	Input Source	VRP Connection	VRN Connection
EXT	Down	External (J1, pins 18 and 20)	J1 pin 20	J1 pin 18
OBH	Middle	Onboard, high common-mode	+AVDD	+2.5V
OBL	Up	Onboard, low common-mode	+2.5V	AGND

In the EXT position, J1 pins 18 and 20 are connected to the ADS1256 reference input.

In the OBH position, the analog power supply is connected to the positive reference input, and the negative reference input is connected to the output of the onboard reference.

In the OBL position, the onboard reference output is connected to the ADS1256 positive reference input pin, and the negative reference input pin is grounded.

Both OBH and OBL provide a +2.5V reference to the ADS1256. The OBL position corresponds to the usual way to connect a reference to the ADS1256, and should be used for most measurements. The OBH position is useful for testing the reference input common-mode sensitivity, which can be important for ratiometric connections.

2.3.4 S5: System Clock Select

This switch selects which of the two available clock sources on the ADS1256EVM will be provided to the ADS1256. The positions of the switch are described in Table 8.

Table 8. System Clock Select Switch

Board Marking	Switch Position	Digital Power Supply Source
XTAL	Left	Onboard 7.68MHz Crystal
EXT	Right	External (J2 pin 17)

3 Usage

This section provides guidelines on using the ADS1256EVM and connecting other systems to it.

3.1 Input Filtering Capacitors

The ADS1256EVM has pads for filtering capacitors on every input pair and for the reference input. Each input pair has pads for two common-mode capacitors and one differential capacitor.

The ADS1256 has a flexible input multiplexer, so these capacitors do not always function as common-mode and differential signal filters. For example, when measuring a single-ended input, the common-mode capacitors act to filter the signal.

The ADS1256EVM is shipped with only a few of the capacitor pads populated. This configuration allows the board to be immediately used to measure both differential and single-ended inputs. As shipped, inputs AIN0 through AIN7 have 10nF differential mode capacitors installed. A differential 1µF capacitor is connected to the reference near the reference pins.

The input filtering capacitors are in relatively large 1210-size packages, in contrast to most of the other passives on the board. These capacitors were designed to be large so that you can easily remove them or replace them with other values. By exercising appropriate care, you can even solder leaded devices to these large pads.

3.2 Serial Interface

The ADS1256 serial interface is connected through 100Ω resistors to the ADS1256EVM serial connector. The resistors help terminate the lines and slow down fast edges that can couple into the part and reduce performance.

The way you connect the ADS1256EVM in a prototype situation will normally be the same as the way you connect it in your final product. See the product datasheet for information on the serial interface of the ADS1256.

3.3 Serial EEPROM

The serial EEPROM is a Microchip 24LC256 32kB type. You can use it for anything you like; the chip is not programmed during manufacturing. Some possible uses include calibration data or board ID information.

Information on communicating with the EEPROM is available from Microchip Technology, Inc.

3.4 Single-Ended vs Differential Signals

The ADS1256 is a differential-input ADC with a flexible multiplexer. The ADS1256 has nine input pins. Without restriction, any of them can be the converter positive input, and any can function as the converter negative input. This flexibility allows the ADS1256 to measure any combination of differential and single-ended signals.

Since the ADS1256 is a differential-input converter and always records its inputs in a bipolar range, the proper way to measure single-ended signals may not be obvious. Here is one method for measuring a 0V to 5V single-ended signal:

1. Connect the signal to one of the ADS1256 input pins.
2. Connect the reference to another of the ADS1256 input pins. The ninth input, AINCOM, is provided for this purpose, but any other input can be used.
3. Set the ADS1256 device gain to 2.
4. Measure between the first input pin and the second input pin. The result will vary from negative full-scale to positive full-scale.

The ADS1256EVM is preconfigured to accept differential signals on input pairs AIN0/1 and AIN2/3; 10nF common-mode filtering capacitors are provided on these channels.

On the ADS1256EVM, the onboard reference is not accessible externally. To connect the reference to an input pin, switch either SW1 or SW2 to the REF position. This connects the reference to AIN0 and AIN2 respectively. You can then measure a single-ended signal on inputs AIN4 to AIN7 or AINCOM as described earlier. (Since AIN1 and AIN3 are grounded in the REF position, these cannot be used as signal inputs.)

3.5 Notes on Optimizing Performance

In our tests, we found that the ADS1256EVM alone—that is, using the onboard reference circuit—is capable of closely approaching, though not matching, the highest possible performance of the ADS1256. This section describes the issues that limit EVM performance, and suggests several ways to increase its performance.

The ADS1256 is unusual among high-resolution delta-sigma ADCs because of the wide range of data rates it offers. A single register setting changes it from a very low-speed, low-noise converter to a relatively high-speed converter. These uses have different circuit requirements.

When low noise is the primary goal, the ADS1256 can be operated in a very low data-rate mode—nominally 2.5 samples per second. The low noise observed in this mode results from the modulator design, the chopper front-end, and averaging together a large number of samples. In this mode, much of the noise is averaged out of the data, and issues such as reference noise become less important. The primary concern at low data rates is then drift and 1/f noise. The onboard reference, based on a REF5025, has a maximum temperature drift of 3ppm/°C. For many applications, this drift will provide an adequate low-noise reference source.

At higher data rates, higher-frequency noise sources are no longer averaged out and begin to be troublesome. These noise sources include the noise inherent in the ADS1256 device itself, which is not reducible, and the reference noise, which may be reduced. Lowering the reference noise is easily done by filtering with large capacitors (as on the ADS1256EVM reference), but this offers diminishing returns, as the ESR of the capacitor limits its effectiveness as a low-pass filter. Beginning with an inherently low-noise reference circuit can be of great benefit here.

Note that large capacitors have increased turn-on settling time, which may be detrimental in some applications. Note also that higher data rate applications are often less affected by drift and 1/f noise.(1)

The ADS1256 is a highly precise converter. Its measurement performance can be degraded by a large number of factors. For example, on the MSP430-based modular EVM motherboard, we noted wide variation in ENOB at certain data rates, sometimes depending on the particular computer that is connected to the fixture. A lower-than-expected ENOB is typically not a fault in the EVM construction, but in numerous possible external factors such as radiated noise and switching power supplies.

(1) An early test board for the ADS1256 employed a 10-farad ultracapacitor to filter the reference noise. Although it filtered the noise very thoroughly, it took over three days following power-up for this capacitor to settle to the proper voltage.

4 Schematic and Layout

This section contains the complete bill of materials, schematic diagram, and printed circuit board (PCB) layout for the ADS1256EVM.

Note: Board layouts are not to scale. These are intended to show how the board is laid out; they are not intended to be used for manufacturing ADS1256EVM PCBs.

4.1 Schematic

The ADS1256EVM schematic is appended to this document.

4.2 Printed Circuit Board Layout

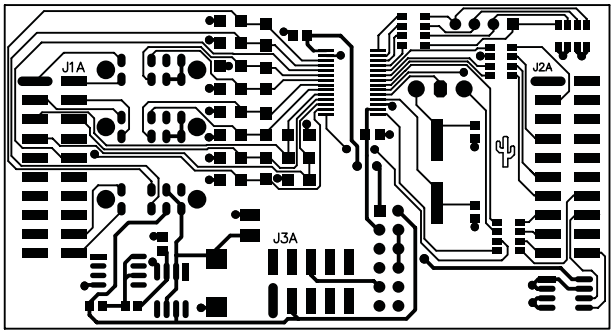


Figure 8. Top Side Layout

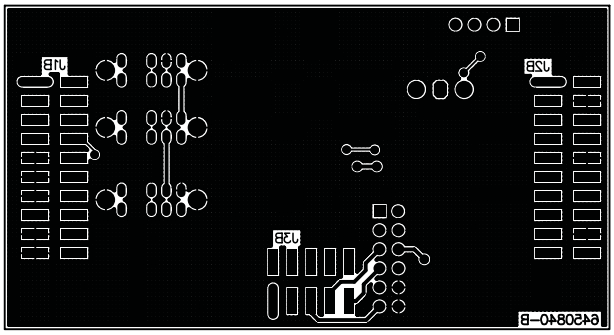


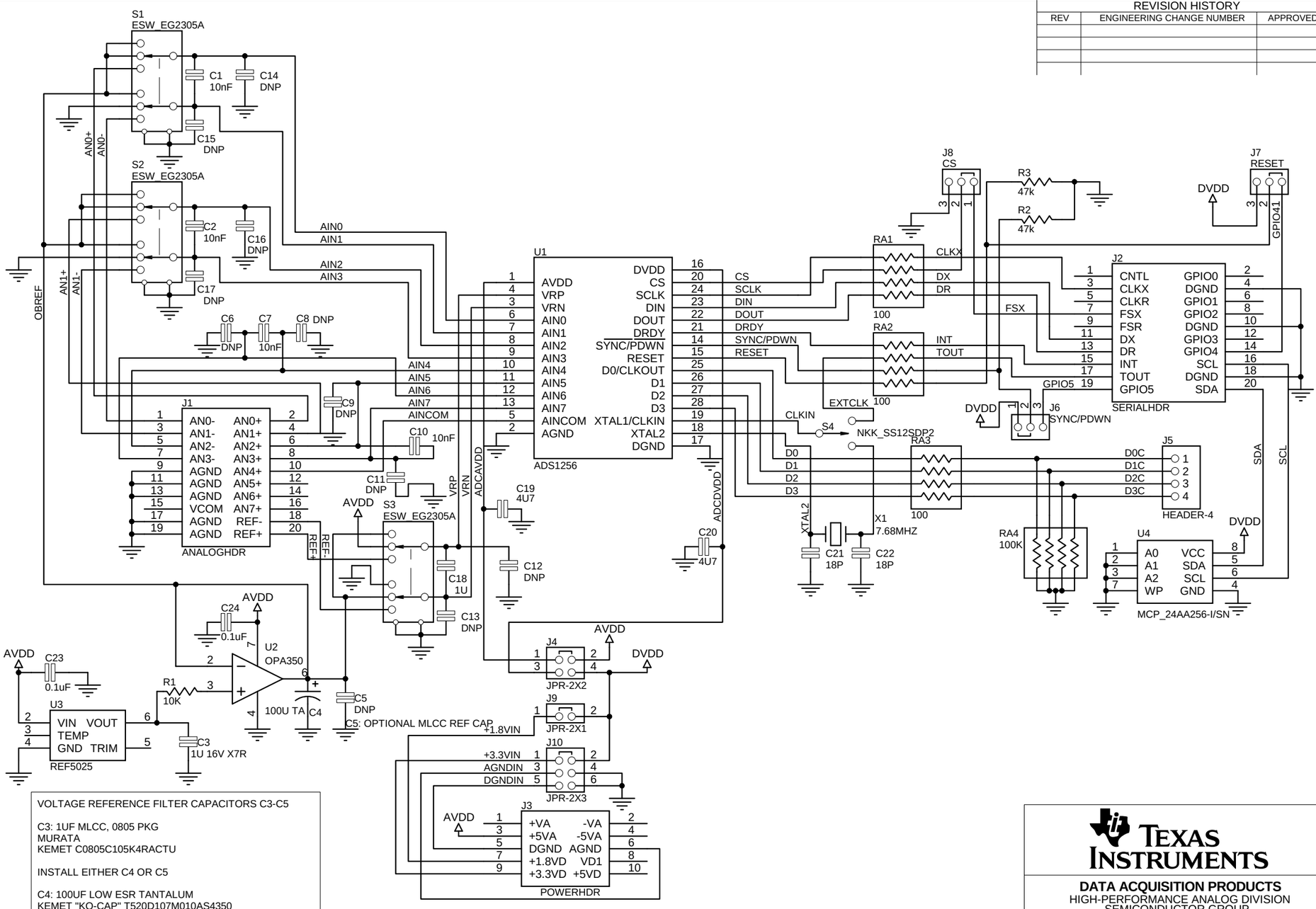
Figure 9. Bottom Side Layout

4.3 Bill of Materials

Table 9. ADS1256EVM Bill of Materials

Reference Designator	Description	Vendor	Part Number
R4	1/10W 5% 10kΩ chip resistor	Panasonic	ERJ–3GEYJ103V
R1	1/16W 1% 24.9kΩ chip resistor	Panasonic	ERJ–3EKF2492V
RA1, RA2, RA3	100Ω 4-position resistor array	CTS	744C083101JTR
RA4	100kΩ 4-position resistor array	CTS	744C083104JTR
C21, C22	18pF ceramic chip capacitor, ±5%, NPO, 0603, 50V	Panasonic	ECJ-1VC1H180J
C3	1μF ceramic chip capacitor, ±10%, X7R, 0603, 16V	Kemet	C0805C105K4RACTU
C18	1μF ceramic chip capacitor, ±10%, X7R, 1206, 25V	TDK	C3216X7R1C105K/0.85
C19, C20	4.7μF ceramic chip capacitor, ±20%, X5R, 0805, 6.3V	TDK	C2012X5R0J475K
C4	100μF tantalum electrolytic capacitor, low ESR type, ±20%, 10V	Kemet	T520D107M010ASE055
C1, C2, C7, C10	100pF ceramic chip capacitor, ±5%, NP, 1206, 50V	TDK	C3216C0G2J101JT
C5, C6, C8, C9, C11–C17	Not installed	–	–
D1, D2	30V 1.5A Schottky barrier diode	Panasonic	MA2Q70500L
X1	Crystal, 7.68MHz	Citizen	HCM49-7.680MABJT
U1	Analog-to-digital converter	Texas Instruments	ADS1256IDB
U2	Operational amplifier	Texas Instruments	OPA350UA
U3	Voltage reference, 2.5V	Texas Instruments	REF5025
U4	EEPROM, I^2C, 256K bits	Microchip	24LC256-I/SN
J1A, J2A	SMT header, 20-pin, dual-row	Samtec	TSM-110-01-L-DV-P
J1B, J2B	SMT socket, 20-pin, dual-row	Samtec	SSW-110-22-F-D-VS-K
J3A	SMT header, 10-pin, dual-row	Samtec	TSM-105-01-L-DV-P
J3B	SMT socket, 10-pin, dual-row	Samtec	SSW-105-22-F-D-VS-K
J5	Header, 4-pin	Samtec	TSW-104-07-L-S
J8, J7, J8	Header, 3-pin	Samtec	TSW-103-07-L-S
J4	Header, 10-pin, dual-row	Samtec	TSM-105-07-L-S
S5	SPDT slide switch	Tyco-Alcoswitch	SLS121PC
S1, S2, S3	DP3T slide switch	E-Switch	EG2305A

REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED



VOLTAGE REFERENCE FILTER CAPACITORS C3-C5

C3: 1UF MLCC, 0805 PKG
MURATA
KEMET C0805C105K4RACTU

INSTALL EITHER C4 OR C5

C4: 100UF LOW ESR TANTALUM
KEMET "KO-CAP" T520D107M010AS4350

C5: 22UF MLCC
MURATA
KEMET
PANASONIC

TEXAS INSTRUMENTS

DATA ACQUISITION PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

ENGINEER **M. ASHTON/ R. ANDERSON**	TITLE **ADS1256EVM**		
DRAWN BY **M. ASHTON**			
DOCUMENT CONTROL NO **6450841**	SIZE **A**	DATE **22 JUN 2007**	REV **C**
SHEET **1** OF **1**	FILE **C:\USERDATA\EVMS\ADS1256\ads1256evm.ddb - ads1256evm.sch**		

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